REMARKS

As a preliminary matter, Applicant requests acknowledgement of the references cited in an Information Disclosure Statement filed on July 17, 2003. A copy of the PTO 1449 form is enclosed.

Claim 5 has been amended to overcome the outstanding 35 U.S.C. § 112 rejection. Withdrawal is requested.

Claims 1-9, 11, 13-14, 16-18, 20-23 and 25-30 stand rejected under 35 U.S.C. § 102 on the basis of Zahir, et al. The claims have been amended to overcome this rejection.

Applicant traverses because Zahir does not disclose (or suggest) "a processor..arranged to execute a plurality of threads on a timeshare basis, the threads being able to change execution mode" as in amended claim 1. The Examiner asserts that Zahir teaches this arrangement, but justifies this conclusion only with the expression "parallel, etc." Parallel processing does not equate to threads executed on a timeshare basis. For example, the third paragraph of the text of the present application notes that "modern processors are usually designed to support multi-tasking, that is, they allow several threads of execution to be processed at what appears to the user to be the same time."

Furthermore, Zahir does not teach that "the number of threads in the second execution mode at any one time is limited, to limit the number of times that the second processor context is preserved and restored." There is no mention in the passages cited by the Examiner of such a limit.

Zahir mentions various forms of context switches. For example, there is a switch from context A or interrupting context to a second context B or interrupting context (column 11, lines 25-30). There is also a switch in context between the application stack and the operating system (column 12, lines 58-64). In none of the situations is there any mention of limiting the number of "threads" in the second execution mode.

Moreover, claim 1 is not obvious over Zahir because neither Zahir nor any other cited document or any combination of cited documents make the limitation of threads in a second execution mode obvious to one of ordinary skill in the art.

The second processor context is designed to be larger than the first processor context in claim 1 of the present application. Therefore, the advantage of limiting the number of times that the second processor context is preserved and stored is clear.

For example, in the present application, page 2 of the description in the second and third paragraph note the disadvantages of preserving the processor context of the parallel processing mode (second execution method). This may consume an undesirably large amount of processor time, and thereby reduce the rate at which tasks can be processed.

Zahir itself makes no mention of threads and cannot alone lead the person already skilled in the art to limit the number of threads in the second execution mode at any one time. There is no disclosure of limiting the number of processes in the second execution mode.

U.S. Patent 6,052,078 (et al) to Flynn discloses multiple threads on a processor. It also discloses occurrences of events in multi-thread management. The events numbered 1 to 16 in column 6 and in column 7 and 8 number (a) to (y) and 1 to 6 can be used to initiate a thread switch. However, none of these relates to limiting the number of threads in a second execution mode at any one time. In fact, it seems from the paragraph bridging columns 5 and 6 that a fixed amount of memory is allocated to each thread (two concurrent threads, are each allocated half of PMCs 84). Furthermore, there is no link between the suspension of execution of a switch until a predetermined number of instructions have been carried out, as in Flynn, and the generated exceptions showing which of two execution modes are used, and the limitation of the number of threads in the second execution mode of claim 1. Rather, Flynn provides a multi-threaded processor including a performance monitor that can individually monitor the performance of multiple concurrent threads when operating in a first mode. The performance monitor can also be configured by software to operate in a second mode in which all event occurrences generated by the processor are monitored collectively (column 10, lines 37 to 45). This mode of the performance monitor does not equate to the execution modes in the present claims or demonstrate changes in execution modes caused by the change of active thread or a change of execution mode of a currently active thread.

U.S. 5,481,719 (Ackerman, et al.) discloses threads in a first and second execution mode (see abstract). This document aims to restore a context during a thread's execution only when necessary (see summary of the invention). However, this document discloses no limit on the number

of threads in the second execution mode. In fact, as explained in column 17, lines 51 to 52 and column 19, lines 55 to 58, once a thread is in the second execution mode (floating point context) it continues in the second execution mode throughout the remainder of its life. Thus, the second processor context is consistently saved for the remainder of that thread, and the number of threads in the second execution mode may gradually increase. This methodology teaches away from the idea now defined in the independent claims of limiting the number of threads in the second execution mode.

Spiller (U.S. 6,047,122) discloses a parallel computer with a plurality of processing elements and a control processor. Although Spiller teaches switching from a scalar mode to a parallel mode, the passages mentioned by the Examiner do not concern limiting the number of threads in the second (parallel) mode.

The rejections of dependent claims 10, 12, 15 and 19 and independent claims 27 and 30 are traversed for the reasons first given. Withdrawal is respectfully requested.

For the foregoing reasons, Applicants believe that this case is in condition for allowance, which is respectfully requested. The examiner should call Applicants' attorney if an interview would expedite prosecution.

Respectfully submitted,

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U.S. PATENT DOCUMENTS

Examiner Initial*		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
		5,481,719	01-02-96	Ackerman et al.	395	700	Sep. 9, 1994

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No
		EP 0 962 856	08-12-99	EP	G06F	9/38	X	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner	Date Considered

*Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.